WHAT IS CLAIMED IS:

1. A parallel computer having a hierarchy structure comprising:

an upper processing unit for executing a parallel processing task in parallel; and

a plurality of lower processing units connected to the upper processing unit through a connection line,

wherein the upper processing unit divides the parallel processing task to a plurality of subtasks, and assigns the plurality of subtasks to the corresponding lower processing units and transfers data to be required for executing the plurality of subtasks to the lower processing units, and

the lower processing units execute the corresponding subtasks from the upper processing unit, and inform the completion of the execution of the corresponding subtasks to the upper processing unit when the execution of the subtasks is completed, and

the upper processing unit completes the parallel processing task when receiving the information of the completion of the execution from all of the lower processing units.

2. A parallel computer having a hierarchy structure comprising:

an upper processing unit for executing a parallel processing task in parallel;

a plurality of intermediate processing units connected to the upper processing unit through a first connection line; and

a plurality of lower processing units connected to the

intermediate processing units through a second connection line,

wherein the upper processing unit divides the parallel processing task to a plurality of first subtasks, and assigns the plurality of first subtasks to the corresponding intermediate processing units, and transfers data to be required for executing the plurality of first subtasks to the intermediate processing units, and

the intermediate processing units divide the first subtasks to a plurality of second subtasks, and assigns the plurality of second subtasks to the corresponding lower processing units, and transfers data to be required for executing the plurality of second subtasks to the lower processing units, and

the lower processing units execute the corresponding second subtasks, and inform the completion of the execution of the second subtasks to the corresponding intermediate processing units when the execution of all of the second subtasks is completed, and

the intermediate processing units inform the completion of the execution of the corresponding second subtasks to the upper processing units when the execution of all of the first subtasks is completed, and

the upper processing unit completes the parallel processing task when receiving the information of the completion of the execution from all of the intermediate processing units.

3. A parallel computer having a hierarchy structure according to claim 1, wherein the lower processing units connected to the connection line are mounted on a smaller area when compared with the upper processing unit, and a signal line through which each

lower processing unit is connected has a smaller wiring capacity, and an operation frequency for the lower processing units is higher than that for the upper processing unit.

4. A parallel computer having a hierarchy structure according to claim 2, wherein the lower processing units connected to the second connection line are mounted on a smaller area when compared with the intermediate processing units connected to the first connection line, and a signal line through which each lower processing unit is connected has a smaller wiring capacity, and an operation frequency for the lower processing units is higher than that for the intermediate processing units.

5. A parallel computer having a hierarchy structure according to claim 3, wherein each of the upper processing unit and the lower processing units has a processor and a memory connected to the processor.

6. A parallel computer having a hierarchy structure according to claim 4, wherein each of the upper processing unit, the intermediate processing units, and the lower processing units has a processor and a memory connected to the processor.

7. A parallel computer having a hierarchy structure according to claim 3, wherein the upper processing unit receives information regarding the completion of the subtask from each lower processing unit through a status signal line.

8. A parallel computer having a hierarchy structure according to claim 4, wherein each intermediate processing unit and the

upper processing unit receives information regarding the completion of the second subtask and the first subtask from each lower processing unit and each intermediate processing unit through a status signal line, respectively.

9. A parallel computer having a hierarchy structure according to claim 3, wherein each lower processing unit comprises a processor, and a memory and a DMA controller connected to the processor.

10. A parallel computer having a hierarchy structure according to claim 4, wherein each intermediate processing unit comprises a processor, and a memory and a DMA controller connected to the processor.

11. A parallel computer having a hierarchy structure according to claim 9, wherein the processor and the DMA controller are connected in a coprocessor connection.

12. A parallel computer having a hierarchy structure according to claim 10, wherein the processor and the DMA controller are connected in a coprocessor connection.

13. A parallel computer having a hierarchy structure according to claim 3, wherein the upper processing unit compresses the data to be required for executing the subtasks, and then transfers the compressed data to the corresponding lower processing units.

14. A parallel computer having a hierarchy structure according to claim 4, wherein the upper processing unit compresses the

data to be required for executing the first subtasks, and then transfers the compressed data to the corresponding intermediate processing units.

15. A parallel computer having a hierarchy structure according to claim 5, wherein each intermediate processing unit compresses the data to be required for executing the second subtasks, and then transfers the compressed data to the corresponding lower processing units.

16. A parallel computer having a hierarchy structure according to claim 4, wherein each intermediate processing unit is a DMA transfer processing unit.

17. A parallel computer having a hierarchy structure according to claim 16, wherein the DMA transfer processing unit is a programmable.

18. A parallel computer having a hierarchy structure according to claim 1, wherein each lower processing unit is mounted with the upper processing unit as a multi-chip module on a board.

19. A parallel computer having a hierarchy structure according to claim 2, wherein each intermediate processing unit and the corresponding lower processing units are mounted with the upper processing unit as a multi-chip module on a board.

20. A parallel computer having a hierarchy structure according to claim 1, wherein each of the upper processing unit and the lower processing units is formed on an independent semiconductor

chip, and each semiconductor chip is mounted as a single multi-chip module.

21. A parallel computer having a hierarchy structure according to claim 2, wherein each of the intermediate processing units, the corresponding lower processing units, and the upper processing unit is formed on an independent semiconductor chip, and each semiconductor chip is mounted as a single multi-chip module.

22. A parallel computer having a hierarchy structure according to claim 1, wherein a structure of the connection line is a common bus connection.

23. A parallel computer having a hierarchy structure according to claim 2, wherein a structure of each of the first connection line and the second connection line is a common bus connection.

24. A parallel computer having a hierarchy structure according to claim 1, wherein a structure of the connection line is a cross-bus connection.

25. A parallel computer having a hierarchy structure according to claim 2, wherein a structure of each of the first connection line and the second connection line is a cross-bus connection.

26. A parallel computer having a hierarchy structure according to claim 1, wherein a structure of the connection line is a star connection.

27. A parallel computer having a hierarchy structure according to claim 2, wherein a structure of each of the first connection line and the second connection line is a star connection.